FACULTY OF ENGINEERING & TECHNOLOGY

Effective from Academic Batch: 2025-26

Programme: **Bachelor of Technology (Computer Science and Design)**

Semester: **III**

Course Code: **102043401**

Course Title: **Digital Fundamentals**

Course Group: **Engineering Science**

Course Objectives:

The objective of this course is to provide a foundation in digital electronics by introducing number systems, binary codes, logic gates, and logic families used in digital information processing. The course develops the ability to analyze, formulate, and simplify Boolean expressions using Boolean algebra and minimization techniques. It also focuses on the design and analysis of combinational and sequential logic circuits using standard components such as adders, multiplexers, flip-flops, counters, and registers. Additionally, the course introduces memory organization and programmable logic devices for digital system design.

Teaching & Examination Scheme:

Contact hours per week			Course Credits	Examination Marks (Maximum / Passing)				
				Theory		J/V/P*		Total
Lecture	Tutorial	Practical		Internal	External	Internal	External	
3	0	2	4	50 / 18	50 / 18	25 / 9	25 / 9	150 / 54

* **J**: Jury; **V**: Viva; **P**: Practical

Detailed Syllabus:

Sr.	Contents	Hours
1	**Introduction:** Binary Numbers, Number base conversion, Octal and Hexadecimal numbers, Binary addition and subtraction using complement method, Binary Codes, Logic Gates, Logic Families: Transistor-Transistor Logic (TTL), Emitter-Coupled Logic (ECL), and MOSFET Logic.	8
2	**Boolean Algebra and Logic Gates:** Basic definition, Axiomatic definition of Boolean algebra, Basic theorem and Properties of Boolean algebra, Boolean functions, Canonical and Standard forms, Logic operations.	5

3	**Simplification of Boolean Functions:** Different types of map method, Sum of product and Product of sum simplification, NAND or NOR implementation, Realizing logic function with gates, Combinational design examples, Don't care condition, Tabulation method.	**7**
4	**Combinational Logic with MSI and LSI:** Binary adders, Binary subtractors, BCD arithmetic, Carry look ahead adder, Digital comparator, Code converters, Magnitude comparator, Encoders, Decoders, Multiplexers, De-Multiplexers, Parity generator and checker.	**8**
5	**Analysis and Design of Sequential Logic Circuits:** Introduction to sequential logic, Flip-Flops, Triggering of Flip-Flops, State machines, Moore model, Mealy model, Analysis of clocked sequential circuits, State reduction and assignments, Flip-Flop excitation tables, Design of counters, Design with state equations, Serial adders, Registers, Shift register, Applications of shift registers, Ripple counters, Timing sequences.	**9**
6	**Memory and Programmable Logic Devices:** Classification of memory, RAM, Memory decoding, Read Only Memory(ROM), PROM, EPROM, EEPROM, Programmable Logic Devices(PLDs), Programmable Logic Array (PLA), Programmable Array Logic(PAL).	**3**
	Total:	**40**

List of Practicals / Tutorials:

1	A. To study operation of various logic gates AND, OR, NOT, NAND, NOR and EX-OR. B. To study NAND/NOR as universal gates.
2	A. Reduce Boolean Expressions to its simplest possible form and implement it using NAND gates. B. Develop a logic circuit depending on the requirement of the given logic problem and implement the circuit using NAND gates into its simplest form.
3	A. Design a combinational logic circuit that gives square of the Two-bit number. B. Design a combinational logic circuit that determines whether given number is prime or non-prime number.
4	A. Design a BCD to Gray code converter & realize it using various logic gates. B. Design a BCD to XS – 3 code converter & realize it using various logic gates.
5	A. Construct the Half Adder and Full Adder using logic gages and verify the truth-table for each. B. Construct the Half Subtractor and Full Subtractor using logic gages and verify the truth-table for each
6	A. Realize 8:1 multiplexer using two 4:1 multiplexer. B. Realize a given logic function using 4:1 Multiplexer and logic gates.

7	A. Implement a Full Adder circuit using 3:8 Decoder. B. Compare two four-bit numbers using a 4-bit Magnitude comparator.
8	Design 3-bit Ripple up counter using Master-Slave JK Flip-flops.
9	Design a synchronous counter using any Flip-flops.
10	Using D-Flip-flops set-up following 4-bit Shift Registers. (i) SISO (ii) PIPO (iii) SIPO (iv) PISO
11	Design a sequence detector using Finite State Machine.
12	A. Introduction to VHDL Code. B. Simulate the full adder using VHDL.

Reference Books:

1	Digital logic and Computer design, M. M. Mano, Pearson Education India, 2016.
2	Digital Fundamentals, Thomas L. Floyd, Edition-11, Pearson.
3	Digital Principles and Applications, Malvino & Leach, McGraw-Hill Education
4	Modern Digital Electronics, R. P. Jain, McGraw Hill Education, 2009.
5	Digital Logic & State Machine Design, David J. Comer, Third Indian Edition, Oxford University Press

Supplementary learning material:	
1	NPTEL Course: NOC: Digital Circuits, IIT Kharagpur, Prof. Santanu Chattopadhyay.
2	Virtual Lab: https://de-iitr.vlabs.ac.in/
3	MultiSim / LogiSim / Electronic Workbench simulator for practical performance

Pedagogy:

- Direct classroom teaching
- Audio Visual presentations/demonstrations
- Assignments/Quiz
- Continuous assessment
- Interactive methods
- Seminar/Poster Presentation
- Industrial/ Field visits
- Course Projects

Suggested Specification table with Marks (Theory) (Revised Bloom's Taxonomy):

Distribution of Theory Marks in %						**R**: Remembering; **U**: Understanding; **A**: Applying; **N**: Analyzing; **E**: Evaluating; **C**: Creating
R	**U**	**A**	**N**	**E**	**C**	
15%	20%	30%	15%	10%	10%	

Note: This specification table shall be treated as a general guideline for students and teachers. The actual distribution of marks in the question paper may vary slightly from above table.

Student Learning Outcomes (SLOs):

Sr.	Student Learning Outcome Statements	%weightage
SLO-1	Apply number systems, binary codes, logic gates, and logic families to represent and process digital information.	**15%**
SLO-2	Analyze and formulate Boolean expressions using Boolean algebra, canonical forms, and logic operations.	**15%**
SLO-3	Simplify Boolean functions using Karnaugh maps and tabulation methods and implement them using logic gates.	**20%**
SLO-4	Design and evaluate combinational logic circuits using MSI and LSI components such as adders, multiplexers, decoders, and comparators.	**20%**
SLO-5	Analyze and design sequential logic circuits including flip-flops, counters, registers, and finite state machines.	**20%**
SLO-6	Explain and apply memory organization concepts and programmable logic devices for digital system design.	**10%**

Curriculum Revision:	
Version:	3.0
Drafted on (Month-Year):	March-2026
Last Reviewed on (Month-Year):	-
Next Review on (Month-Year):	April-2029