इलेक्ट्रॉनिकी एवं सूचना प्रौद्योगिकी मंत्रालय
MINISTRY OF ELECTRONICS AND INFORMATION TECHNOLOGY

CVM UNIVERSITY

ADIT
A D PATEL INSTITUTE OF TECHNOLOGY

NATIONAL FACULTY DEVELOPMENT PROGRAM ON

Multidisciplinary Applications of Semiconductor Technologies using EDA Tools

20th – 24th April, 2026

In-Association With:

CoreEL Technologies – Enabling Excellence
ISTE – Indian Society for Technical Education
इसरो isro
eInfochips
Institution's Innovation Council (Ministry of HRD Initiative)
The Institution of Engineers (India)
Chips to Startup Programme
sandeepani

Organized By:

Department of Electronics and Communication Engineering

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4 QUALITY EDUCATION
9 INDUSTRY, INNOVATION AND INFRASTRUCTURE
11 SUSTAINABLE CITIES AND COMMUNITIES

ABOUT CVM UNIVERSITY

Charutar Vidya Mandal University (CVMU) established in the year 2019 as a largest self- financed state private university with a prime objective of imparting quality education for current and future needs of individual, society and the Nation. The CVM University offers programs in more than nine academic disciplines. The initial size of the CVM University is largest among all private universities of Gujarat and well-qualified faculty members and non- academic staff members are the part of the CVM University.

ABOUT INSTITUTE

A. D. Patel Institute of Technology (ADIT), New Vallabh Vidyanagar, an Institution of the Charutar Vidya Mandal(CVM) University, established in 2000 with a commitment to delivering quality education in emerging areas of engineering and technology. Spread across a scenic 40-acre eco-friendly campus near Vitthal Udyognagar, ADIT offers state-of-the-art infrastructure, highly qualified faculty, and a techno-scientific environment that promotes holistic learning. Guided by its vision of pioneering excellence in learning, knowledge, and self-realization, the institute is dedicated to providing globally relevant, value-added education in the techno-management domain. Through a strong quality policy, ADIT ensures academic excellence by fulfilling academic requirements, recruiting competent and self-motivated faculty, fostering parent–administration collaboration, and implementing international quality management systems to prepare scholars for meaningful contributions to the global economy.

ABOUT EC DEPARTMENT

The Department of Electronics and Communication Engineering is dedicated to achieving academic distinction and research excellence in advanced electronics, communication systems, and emerging technologies. The program is structured to produce industry-ready and research-driven professionals equipped with strong analytical abilities, technical expertise, and ethical integrity. Aligned with its vision of fostering innovative, rational, and ethically grounded engineering practices, the department delivers a robust curriculum integrating fundamental theory with hands-on experimentation, design, and system-level implementation. It cultivates a dynamic and research-oriented academic ecosystem that promotes critical thinking, problem-solving skills, interdisciplinary competence, and holistic professional development to meet global technological challenges.

ABOUT FDP

The Faculty Development Program (FDP) provides comprehensive, industry-oriented exposure to the semiconductor and VLSI ecosystem—from device fundamentals to ASIC signoff and tape-out. The program covers the global semiconductor supply chain, device fabrication, assembly/packaging, design houses, and India's Semiconductor Mission, highlighting academic and industry collaboration opportunities. Participants will revisit core semiconductor devices (Diode, BJT, MOSFET), sensor technologies, and TCAD-based 2D/3D device simulations. The FDP includes Digital VLSI Design Flow (RTL to GDSII), Verilog HDL modeling, combinational and sequential design, verification using Synopsys tools, synthesis, timing analysis, and backend implementation. It also covers Analog and Mixed-Signal IC design using Cadence and Siemens EDA platforms, including schematic design, simulation, layout, DRC/LVS/PEX, and post-layout validation. The program further emphasizes ASIC signoff methodologies, yield and reliability considerations, and industry best practices for tape-out, complemented by a guided cleanroom visit and insights into key fabrication processes such as lithography, etching, and deposition.

Overall, the FDP delivers a holistic, end-to-end understanding of semiconductor devices, IC design, verification, physical implementation, and signoff aligned with current industry standards.

KEY HIGHLIGHTS OF THE FDP

1. **Diverse Tool Training:** Hands-on sessions covering major EDA industry players: Synopsys, Cadence and Siemens EDA.
2. **End-to-End Design Flow:** Coverage of the entire VLSI spectrum and RTL to GDSII.
3. **Industry Immersive Experience:** Industry Connect Day visit to the **ISRO Foundry**, providing a rare look at clean room processes, lithography, and etching
4. **Specialized Content:** Focus on India's Semiconductor Mission and the role of semiconductors in strategic sectors like space and defense.

RELEVANCE TO CURRICULUM/RESEARCH/INDUSTRY

Bridges basic electronics with advanced system design by integrating Verilog and RTL into coursework. Introduces TCAD/device simulation and material properties for research in device physics and sensors. Enables knowledge transfer from industry experts (ISRO, eInfochips, CoreEL) to keep academics relevant, while preparing learners for the "RTL to GDSII" flow and supporting India's semiconductor mission.

TARGET AUDIENCE

- Faculty members
- Research scholars
- Industry and Academic professionals

REGISTRATION

Link : https://forms.gle/hfBJrmeGVZMxvWN69

Registration Fees:

- CVMU Faculty: ₹500
- Faculty from Other Organisation: ₹700

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Program Schedule of

National FDP on Multidisciplinary Applications of Semiconductor Technologies using EDA tools

Session date/time	Topics covered	Key Concepts/Content
20/4/26	Inaugural session from 9:30 to 10:00 am	
20/4/26	High Tea from 10:00 am to 10:15 am	
Day - 1	**Semiconductor Foundations & Cross-Domain Relevance**	
20/4/26 Session -1: Time: 10:15 am to 11:45 am	Introduction to Semiconductor Ecosystem & India's Semiconductor Mission	Global semiconductor supply chain. Overview of Wafer Fab, Assembly/Packaging, and Design Houses. Importance of semiconductors in the digital economy and strategic sectors. India's Semiconductor Mission and its objectives. Opportunities for academic research and industry collaboration.
20/4/26 Session -2: Time: 12 to 1pm	Semiconductor Devices & Sensor Technologies Across Engineering Domains	Review of basic devices: Diode, BJT, and MOSFET structure and operation. Introduction to various sensor types (MEMS, Chemical, Temperature, Pressure). Applications in: Food Tech (moisture, gas sensing), Chemical (process control), Automobile (LIDAR, pressure), Mechanical (strain, vibration), Electrical/IT (power devices, memory).
20/4/26 Session -3: Time: 2 pm to 4pm	Hands-on: Basics of TCAD / Device Simulation	Introduction to Technology Computer-Aided Design (TCAD). Simulating 2D/3D device structures. Setting up and performing a basic MOSFET I-V characteristic simulation and understanding the link between material properties and device performance.
Day - 2	**Digital VLSI System design using Synopsys**	
21/4/26 Session -1: Time: 9:30 am to 11am	RTL Design using Verilog	Overview of VLSI Design Flow (RTL to GDSII), Introduction to Verilog HDL,Modeling Styles: Behavioral, Dataflow, Structural, Blocking vs Non-blocking Assignments, Combinational Circuit Design (Adder, MUX, Decoder, ALU basics),Sequential Circuit Design (Flip-Flops, Counters, FSM),Coding Guidelines for Synthesizable RTL, Demonstration in Linux Environment
21/4/26 Session -2: Time: 11:15 am to 12:30pm	Functional Verification & Simulation	Importance of Verification in Digital Design, Testbench Architecture and Stimulus Generation, Writing Self-checking Testbenches, Simulation Flow using Synopsys VCS, Waveform Analysis and Debugging using Synopsys Verdi, Practical Demonstration of RTL-to-Simulation Flow
21/4/26 Session -3: Time: 2 pm to 4pm	RTL Synthesis & ASIC Flow Overview	Concept of Synthesis, RTL to Gate-Level Netlist Conversion, Technology Libraries, Timing Constraints (SDC Basics), Area, Timing & Power Reports, Introduction to Backend Flow (Floorplanning, Placement, CTS, Routing), Overview of GDSII Generation

Day - 3	Analog and Digital Design using Cadence tools	
22/4/26 Session -1: Time: 9:30 am to 11am	Digital Design using Cadence Tools	Overview of Semiconductor & VLSI Design Flow • Frontend vs Backend Design • RTL to GDSII Flow • Introduction to Cadence Digital Tool Chain • Overview of Standard Cell Libraries • Introduction to Timing Concepts (Setup, Hold, Clock)
22/4/26 Session -2: Time: 11:15 am to 12:30pm	RTL Coding Best Practices	RTL Coding Best Practices • Importing Verilog into Cadence Environment • Functional Simulation • Synthesis using Cadence Genus • Timing Constraints (Basic SDC) • Area & Timing Reports • Gate-Level Netlist Generation Hands-on: • Synthesize a simple module (Adder / ALU / Counter) • Generate timing and area report • Analyze critical path
22/4/26 Session -3: Time: 2 pm to 4pm	Digital Design using Cadence Tools	Introduction to Physical Design • Floorplanning Basics • Placement & Clock Tree Synthesis • Routing Concepts • DRC & LVS – Conceptual Overview • Power, Area & Timing Optimization • Introduction to GDSII Generation
Day - 4	**Industry Connect Day - ISRO Foundry Visit**	
23/4/26	Introduction to ISRO's Foundry & Strategic Role, Foundry Tour and Fabrication Process Overview	Guided tour of the clean room and process areas (as permitted). Observation/discussion on key fabrication steps: Lithography, Etching, and Deposition. Specific challenges in manufacturing for space applications (e.g., vacuum, thermal cycling). Fabrication Equipment (On-site observation)

Day - 5	Custom IC Design using Siemens EDA	
24/4/26 Session -1: Time: 9:30 am to 11am	Siemens Custom IC Design and Simulation	Introduction to Siemens EDA Ecosystem, Custom IC Design Flow, Schematic Capture and Simulation Setup, Device Characterization, Analog/Mixed Signal Simulation Concepts, Debugging & Convergence Techniques
24/4/26 Session -2: Time: 11:15 am to 12:30pm	Signoff – DRC/LVS and Parasitic Extraction	Importance of Signoff in ASIC Design Flow, Design Rule Checking (DRC), Layout vs Schematic (LVS) Verification, Parasitic Extraction (PEX) Concepts, Yield and Reliability Considerations
24/4/26 Session -3: Time: 2 pm to 4pm	Calibre Signoff Demonstration	End-to-End Signoff Flow Demonstration, Running DRC/LVS on Sample Layout, Debugging DRC/LVS Errors, Post-Layout Analysis, Industry Best Practices for Tape-Out
24/4/26 Time: 4pm	Valedictory	Feedback, Certification & Closing Remarks